Development of an Open Speech Signal Processing Platform

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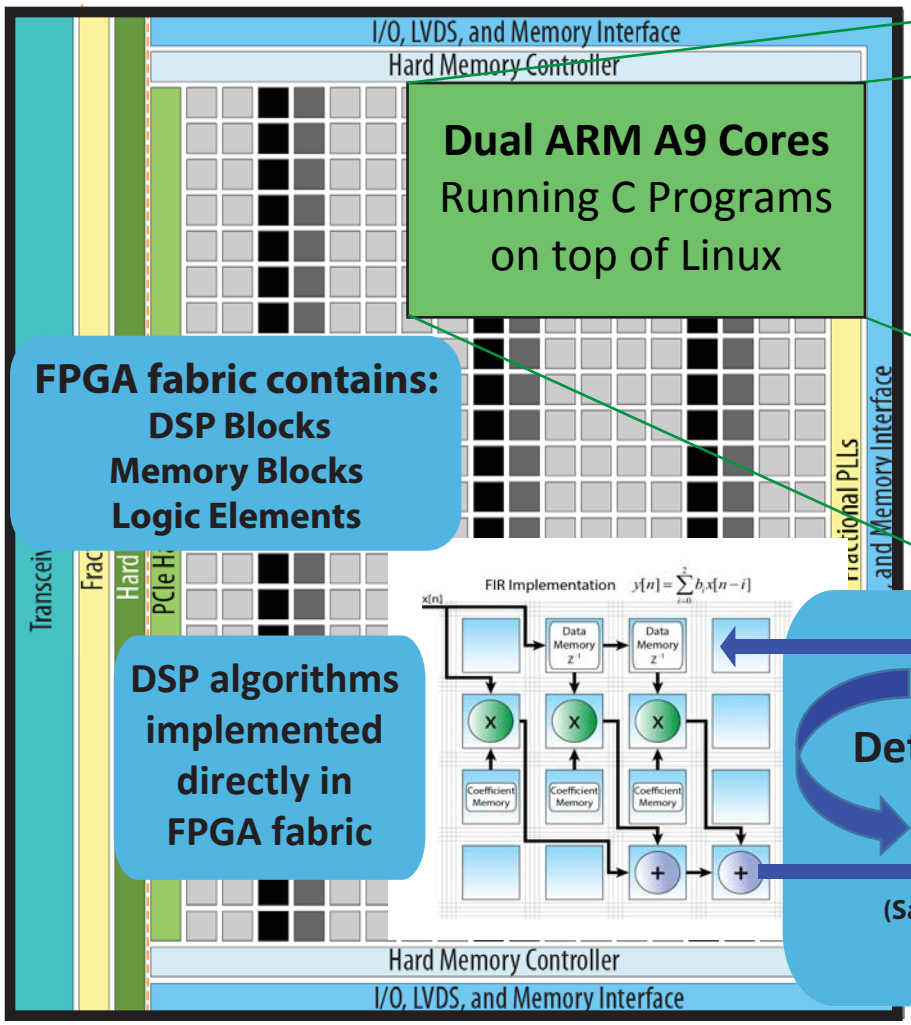
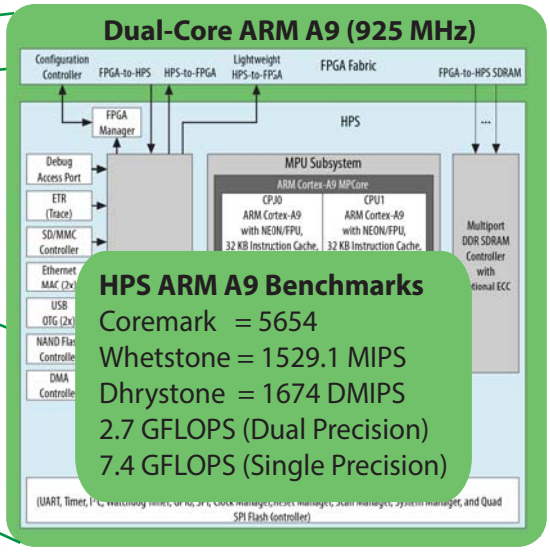
OpenSpeechTools.com

flatearth

The Open Speech Signal Processing Platform will be based on Altera/Intel's Cyclone V SoC FPGAs

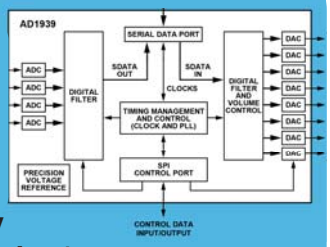




HPS ARM A9 Benchmarks
Coremark = 5654
Whetstone = 1529.1 MIPS
Dhrystone = 1674 DMIPS
2.7 GFLOPS (Dual Precision)
7.4 GFLOPS (Single Precision)

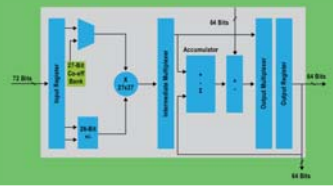
Low Deterministic Latency

Audio Codec

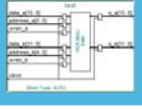


Audio Latency
(Sample Rate Dependent)
63 usec @ 48 KHz
150 usec @ 20 KHz

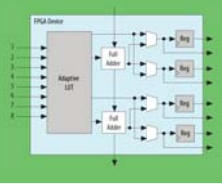
DSP Blocks (112)
27x27 Multipliers and
64-bit Accumulators



Memory Blocks (557 M10K)
M10K = 10 kilobits (Kb) blocks
Total Memory = 5.7 Mbits
1Kx10, 512 x20
Dual Port Memory



Logic Elements (110K LEs)
8 input Lookup Tables
Full Adders



Theoretical Peak Performance (CPU+FPGA)[3]

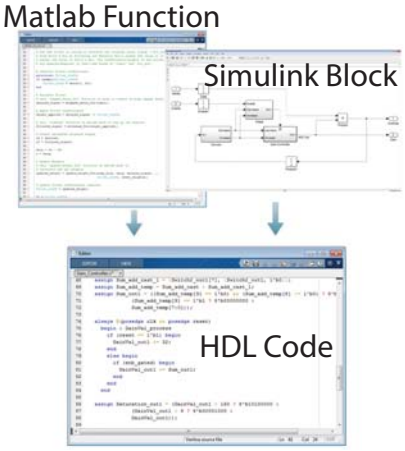
Int16: 149.5 GOPS (44.56 GOPS/W); Int32: 40.99 GOPS (13.23 GOPS/W)
SPFP: 45.96 GFLOPS (8.51 GFLOPS/W); I/O Bandwidth: 69.18 GB/sec

[3]Comparative Analysis of Present and Future Space Processors with Device Metrics;
Military and Aerospace Programmable-Logic Devices Conference, San Diego, CA, May 2014

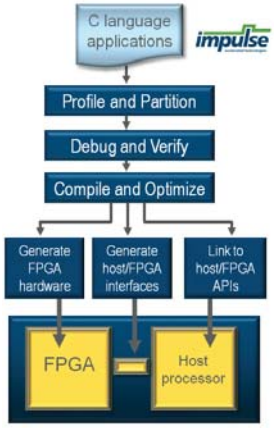
The platform will support three software languages.

1. **Matlab** to target DSP blocks in signal processing path in FPGA fabric.
2. **C** (Impulse C and OpenCL) to target software on ARM CPUs and DSP blocks in FPGA fabric.
3. **VHDL** (and Verilog) to create optimal DSP architectures in FPGA fabric and BSP interfaces.

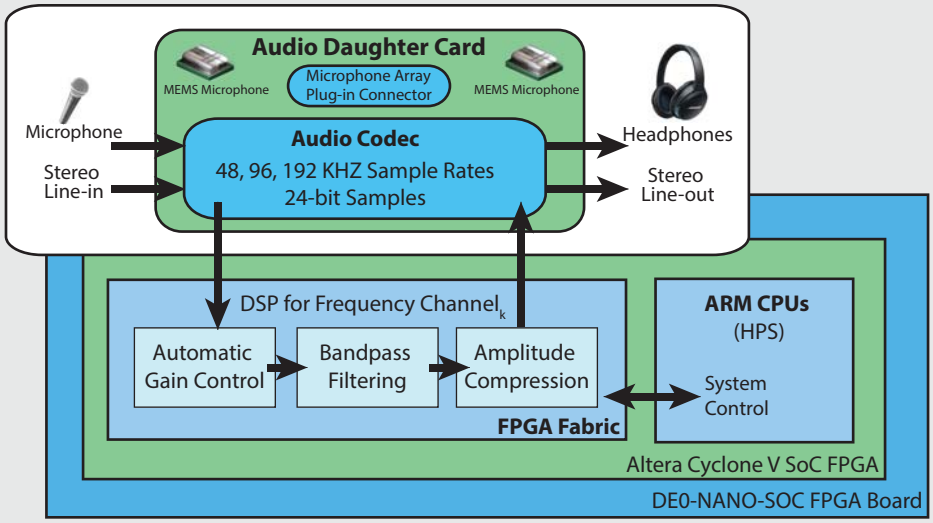
Matlab HDL Coder



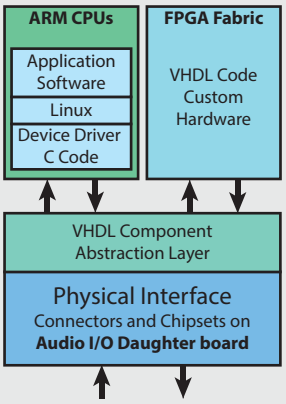
Impulse C and OpenCL



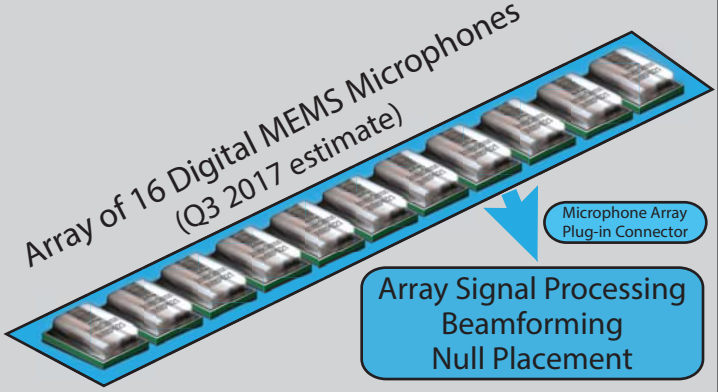
Example Signal Processing Chain



Software Stack



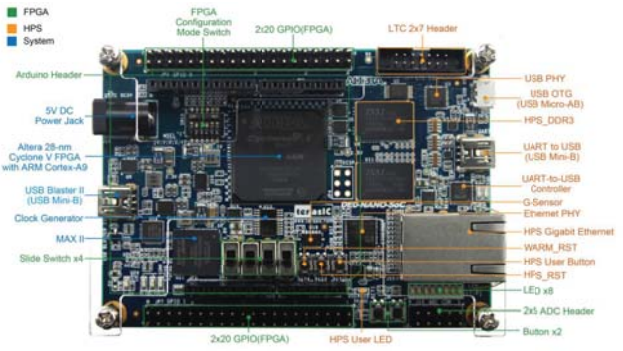
C programs interact with custom VHDL components via Linux device drivers.



First Resource Available (Q1 2017)

Daughter Card that will plug into the DE0-NANO-SOC board that contains:

1. Audio Codec with microphone and stereo line-in inputs.
2. Connector that will accept an array of 16 digital MEMS Microphones.
3. Headphone and stereo line-out outputs.



FPGA Roadmap

Arria 10 is Altera/Intel's midrange FPGA
1.5 TFLOPS single-precision floating-point (SPFP)
1.5 GHz ARM A9 Cores
1,688/1,688 Hardened SPFP Multiplers/Adders
2,133 M20K Memory Blocks
660K Logic Elements (LEs)